REMARKS/ARGUMENTS

Claims 1-15 are pending. Claims 1, 8, and 13 have been amended. Claims 16-20 have been added. Support for the new and amended claims is found in the specification. No new matter has been added.

In summary of the Office Action of December 2, 2005, the Examiner has:

I. Rejected claims 1-4, 6, 7, and 13-15 under 35 U.S.C. § 103(a) as being unpatentable over Cantone et al., U.S. Patent No. 5,594,657, ("Cantone"); in view of IEEE Paper "On Area/Depth Trade-Off in LUT-based FPGA Technology Mapping," authored by Cong and Ding, ("Cong and Ding"); and in view of Nasu, U.S. Patent No. 6,088,262, ("Nasu"); and

II. Rejected claims 8-12 under 35 U.S.C. § 103(a) as being unpatentable over Cantone, in view of Cong and Ding, Nasu, and "Structural Gate Decomposition for Depth-Optimal Technology Mapping in LUT-based FPGA Designs," authored by Cong and Hwang, ("Cong and Hwang").

The applicants respectfully traverse these rejections.

I. Rejection of claims 1-4, 6, 7, and 13-15

Claim 1, as amended, recites in part:

> optimizing the selected netlist based on the corresponding mapping netlist; and performing a technology mapping on the selected netlist after optimizing.

The Applicants respectfully submit that the none of the cited references disclose or suggest at least these elements.

As recited by the claim 1, the selected netlist is one of the first or second alternative netlists obtained from synthesis. The cited portion of claim 1 calls for optimizing this selected netlist based on a corresponding mapping netlist, which is obtained by previously performing a technology mapping of the netlist. An additional technology mapping is then performed on this optimized selected netlist. In summary, the results of a later technology mapping are used as feedback to optimize the output of an earlier synthesis stage. The resulting optimized output is then reprocessed by another technology mapping.

None of the cited references disclosure or suggest "optimizing the selected netlist based on the corresponding mapping netlist," or using the results of a later technology mapping are used as feedback to optimize the output of an earlier synthesis stage; and then "performing a technology mapping on the selected netlist after optimizing," or reprocessing the optimized synthesis results with another technology mapping.

The Examiner states that Cantone does not disclose or suggest performing technology mapping on first and second alternative netlists or selecting between the resulting first and second mapping netlists based on design criteria. As a result, Cantone cannot disclose or suggest "optimizing the selected netlist based on the corresponding mapping netlist; and performing a technology mapping on the selected netlist after optimizing," as these elements require technology mapping as a prerequisite.

Cong and Ding discloses an algorithm for producing "a set of mapping solutions with smooth area and depth trade-off for a given design." (Abstract; p.138, second paragraph). Cong and Ding produce a single synthesis or gate configuration of the design. (p.138, second paragraph). A set of different technology mappings are then generated from this single gate configuration.

Thus, Cong and Ding discloses producing a multiple mapping solutions for a single gate configuration. However, Cong and Ding does not disclose or suggest using the results of a mapping solution to modify the underlying gate configuration, or synthesis, a design.

The Examiner cites Cong and Ding as disclosing "remapping for area-minimization." However, this remapping is to generate additional mapping configurations. "We then re-map the resulting network to obtain an area-minimized mapping solution with bounded depth." (p.138, second paragraph). This remapping does not change the gate configuration, or synthesis, of the design. This is clearly shown in figures 2(a), 2(b), and 2(c). In these figures, a single gate configuration is shown with different technology mappings, such as a depth-optimal mapping in figure 2(b) and an area-optimal mapping in figure 2(c). Despite the differences in the mapping configurations, these figures clearly show that the underlying configuration of gates is identical.

Because Cong and Ding does not disclose or suggest using the results of technology mapping to modify a previously determined gate configuration, Cong and Ding does not disclose or suggest "optimizing the selected netlist based on the corresponding mapping netlist," let alone further "performing a technology mapping on the selected netlist after optimizing," as recited by claim 1.

Moreover, the Examiner has cited to Nasu as disclosing a digital signal processing block. In light of the Examiner's reversal of the findings of allowability in the Office Action of March 11, 2005, the Applicants have amended claim 1 to remove limitations regarding digital signal processing blocks. Therefore, the Applicants submit that the citation of this reference is moot with regards to claim 1.

Because none of the cited references disclose or suggest "optimizing the selected netlist based on the corresponding mapping netlist; and performing a technology mapping on the selected netlist after optimizing," the Applicants respectfully submit that claim 1 and dependent claims 2-4, 6, 7, 16, and 19 are patentable.

Claim 13, as amended, recites in part:

> after the first technology mapping, performing a synthesis optimization on the netlist; and
> after the synthesis optimization, performing a second technology mapping on the netlist

The Applicants respectfully submit that claim 13 is patentable over the cited references for reasons similar to those set forth above.

Cantone does not disclose or suggest performing a synthesis optimization on the netlist after performing the first technology mapping and then performing a second technology mapping on the optimized netlist.

Similarly, there is nothing in Cong and Ding that discloses or suggests optimizing synthesis, which changes the gate configuration, after performing a technology mapping. Moreover, Cong and Ding do not disclose or suggest then performing a second technology mapping on the optimized netlist.

Moreover, the Applicants respectfully submit that Nasu is relevant to claim 13, as claim 13 has been amended to remove any recitation of digital signal processing blocks.

Because none of the cited references disclose or suggest all of the limitations of claim 13, the Applicants respectfully submit that claim 13 and dependent claims 14, 15, 18, and 20 are patentable.

II. Rejection of claims 8-12

Claim 8, as amended, recites in part:

> optimizing the selected netlist based on results of a technology mapping of the first alternative netlist and the second alternative netlists; and
> performing a technology mapping on the selected mapping netlist after optimizing.

The Applicants respectfully submit that the none of the cited references disclose or suggest at least these elements.

The Applicants respectfully submit that claim 8 is patentable over the cited references Cantone, Cong and Ding, and Nasu for reasons similar to those set forth above.

Similarly, Cong and Hwang does not disclose or suggest "optimizing the selected netlist based on results of a technology mapping of the first alternative netlist and the second alternative netlists; and performing a technology mapping on the selected mapping netlist after optimizing," as recited by claim 8. Although Cong and Hwang does disclose using synthesis to determine different structural gate decompositions for a design, Cong and Hwang, like the other cited references, does not disclose using the results of a technology mapping of different alternative netlists to optimize a selected netlist.

Because none of the cited references disclose or suggest all of the limitations of claim 8, the Applicants respectfully submit that claim 8 and dependent claims 9-12, and 17 are patentable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

Jonathan M. Hollander
Reg. No. 48,717

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300

Attachments
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